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# Effects of Annealing Conditions on Charge Loss Mechanisms in MOCVD $Ba_{0.7}Sr_{0.3}TiO_3$ Thin Film Capacitors

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***Abstract***

*The leakage and dielectric relaxation currents of MOCVD $Ba_{0.7}Sr_{0.3}TiO_3$ thin films with Pt electrodes after post top electrode anneals in oxygen and forming gas (95% Ar, 5% $H_2$) were investigated. The Schottky barrier height for thermionic emission of electrons from the cathode varied depending on annealing conditions. The electrically measured barrier height of 0·67 eV in the as deposited film significantly increased to 1·29 eV by annealing at 550°C for 15 min in oxygen, while the magnitude of the relaxation currents were only slightly affected. A subsequent anneal at 400°C in forming gas for 20 min decreased the barrier height to 0·92 eV and increased the dielectric relaxation currents by an order of magnitude. Re-annealing in oxygen at 400°C for 20 min improved the leakage but still resulted in an estimated 28% charge loss due to the slow polarization currents for the large ($10^4$ μm$^2$) unpassivated planar capacitors used in this study.* © *1999 Elsevier Science Limited. All rights reserved*

*Keywords*: interfaces, dielectric, electrical properties, capacitors.

## 1 Introduction

Barium strontium titanate (BST) is currently being considered for use as the storage node dielectric for future dynamic random access memories (DRAMs). The high dielectric constant of BST offers the potential of producing denser memories with simpler capacitor structures than those fabricated with conventional silicon dioxide and/or silicon nitride dielectrics. Integration of a high dielectric constant material into a standard CMOS process flow subjects the capacitor to various ambients during processing which may degrade the electrical properties of the capacitor.[1] One important consideration is the effect of hydrogen containing ambients, which are commonly used to control transistor $SiO_2$/Si interface states, on the leakage and relaxation currants in BST thin films. Hydrogen containing ambients have been shown to degrade electrical properties, such as leakage and remnant polarization, in perovskite titanate dielectrics.[2,3] In this paper, we investigate the effects of oxygen and forming gas (95% Ar, 5% $H_2$) post top electrode anneals on the leakage and dielectric relaxation currents in $Ba_{0.7}Sr_{0.3}TiO_3$ thin films. The field and temperature dependence of the leakage currents followed a Schottky-like emission model with the effective barrier height depending on annealing conditions. Both the relaxation currents and leakage increased with forming gas anneals. Re-annealing in oxygen at 400°C improved the leakage but still resulted in an estimated 28% charge loss due to the slow polarization currents for the large ($10^4$ $\mu$m$^2$) unpassivated capacitors used in this study.

## 2 Experimental

Polycrystalline $Ba_{0.7}Sr_{0.3}TiO_3$ thin films with thickness varying from 8 to 150 nm were prepared

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by metal–organic clinical vapor deposition (MOCVD).[4] The MOCVD BST thin films were deposited on $Si/SiO_2$ substrates with sputtered Pt base electrodes. Pt top electrodes were formed by sputtering a blanket Pt layer and patterned by photolithography. Current measurements were made using an HP4140B pico ammeter. For each sample, the charging current resulting from a voltage step was monitored for 1000 s. An initial voltage of 0·2 volts was used and the voltage was stepped in 0·2 volt increments up to a voltage resulting in an applied field of 1 MV cm$^{-1}$. After each voltage step the capacitor was shorted and the discharging currents recorded for a period of 1000 s. The as deposited samples were annealed at 550°C for 15 min in 1 atm $O_2$. Subsequent anneals were done at 400°C for 20 min in 1 atm forming gas (95% Ar, 5%, $H_2$) and then the samples were re-annealed at 400°C for 20 min in $O_2$. After each anneal, a fresh capacitor was used for the electrical measurements.

## 3 Results and Discussion

### 3.1 Leakage current

The conduction mechanism for charge transport through metal–BST–metal thin film capacitors is dominated by thermionic emission of electrons over an interfacial Schottky barrier whose properties depend on the electrode material and deposition conditions.[5] The metal–BST–metal structure consists of two back-to-back Schottky barriers. Assuming the current flow is controlled by the reversed biased Schottky barrier, the temperature and field dependence of the leakage current is given by[5,6]

$$J_L = A^{**}T^2 \exp\left(\frac{-W_B}{kT}\right) \exp\left(\frac{q}{kT}\sqrt{\frac{qV}{4\pi d\varepsilon}}\right) \quad (1)$$

where $A^{**}$ is the effective Richardson's constant, which incorporates carrier mobility, $T$ the temperature, $V$ the applied voltage, $\varepsilon$ the permittivity (which may be different from the static permittivity), $q$ the electronic charge, $d$ the depletion layer width, and $k$ is Boltzmann's constant. The 30 nm films used in this study are completely depleted and thus, the depletion width equals the film thickness[7,8] and eqn (1) may also be written in terms of the applied field.[5] If the conduction mechanism is thermionic emission, plots of $\log(J/T^2)$ versus $1/T$ and $\log(J)$ versus $\sqrt{V}$ yield straight lines. The barrier height, $W_B$, is then extracted from either the slopes or intercepts of the temperature and field dependence Schottky plots.[5,8] Figure 1 shows the field dependence plotted as $\log(J)$ versus $\sqrt{V}$ for 30 nm MOCVD BST with Pt electrodes under various annealing conditions at 296 K. For all annealing conditions, good linear fits are obtained above a threshold voltage even though the leakage through the films may differ by as much as eight orders of magnitude. The threshold voltage is seen to shift to lower voltages with increasing leakage current (lower effective barrier height). The leakage current of the as deposited film at 1 volt is $2{\cdot}8\times10^{-5}$ A cm$^{-2}$ which is reduced to $1{\cdot}6\times10^{-9}$ A cm$^{-2}$ after annealing at 550°C for 15 min in $O_2$. A subsequent anneal at 400°C in forming gas for 20 min increases the leakage by an order of magnitude at 1 volt. Re-annealing at 400°C for 15 min in $O_2$ again

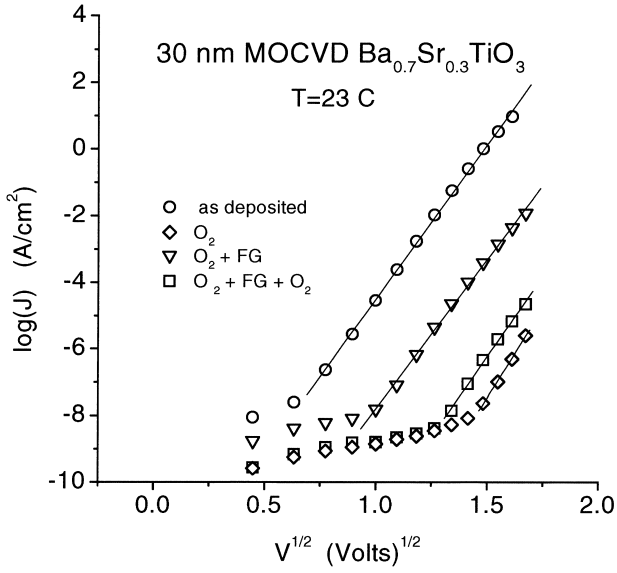


**Fig. 1.** Field dependence for 30 nm MOCVD BST with Pt electrodes under different annealing conditions at 296 K. As deposited, annealed at 550°C for 15 min in $O_2$ subsequent anneal at 400°C for 20 min in forming gas, and re-annealed at 400°C for 20 min in $O_2$.

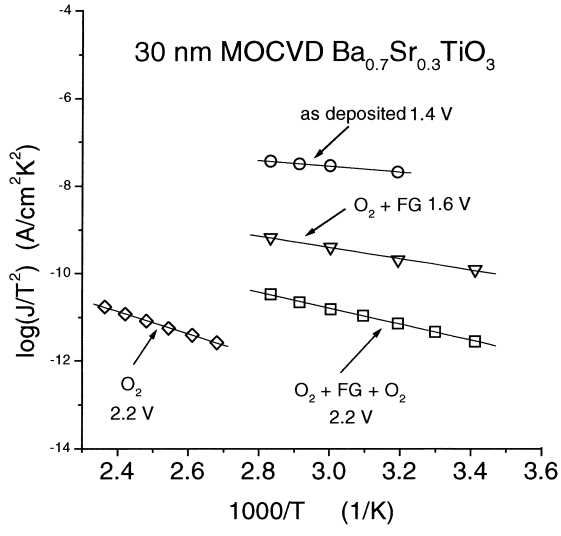


**Fig. 2.** Temperature dependence for 30 nm MOCVD BST with Pt electrodes under the same annealing conditions as in Fig. 1. The applied voltage in the temperature dependence measurement varied from 1·4 to 2·2 volts depending on annealing condition.

improves the leakage resulting in a current density of $2\times10^{-9}$ A cm$^{-2}$. Figure 2 shows the temperature dependence plotted as $\log(J/T^2)$ versus $1000/T$ for 30 nm MOCVD BST with Pt electrodes. As shown in Fig. 2, the applied voltage was varied from 1·4 to 2·2 volts and was chosen such that, for a given annealing condition, the leakage current was in the Schottky regime (above the knee in Fig. 1) but not too large as to cause excessive leakage currents or resistance degradation during the temperature dependence measurements. Table 1 shows the barrier heights for different annealing conditions which were extracted from the field and temperature Schottky plots. The voltage that was applied for the temperature dependence measurement is also listed. The barrier height varies from 0·67 eV for the as deposited film to 1·29 eV after annealing at 550°C for 15 min in $O_2$. The Schottky barrier height for an ideal metal–semiconductor system is the difference between the work function of the metal and the electron affinity of the semiconductor, $W_B = \Phi_M - q\chi$. The exact values for the electron affinity of the BST solid solution are not known but it is expected to be close to that of $SrTiO_3$ where $q\chi = 4{\cdot}1\ eV$.[5] The work function for a clean Pt surface in a vacuum is 5·6 eV[6] yielding an expected ideal barrier height of about 1·5 eV. The measured barrier heights, especially in the as deposited and forming gas annealed samples, are much smaller than this value. Possible reasons for the lower barrier height, and its dependence on annealing condition, will be discussed below. It should be noted that if the standard Schottky expression[eqn (1)] is used, parameters other than the barrier height extracted from the data analysis are typically unrealistic. Recently, a modified Schottky expression derived by Simmons[9] has been used which yield better values for the effective Richardson's constant and permittivity.[10]

No variation with annealing condition would be expected for an ideal Schottky barrier system where the barrier height is determined solely by the metal work function and the electron affinity of the semiconductor. However, in a non ideal Schottky barrier interface states, deep level traps, and fixed interfacial charge[5,6,11,12] can modify the barrier height resulting in an effective barrier that is sensitive to annealing, deposition conditions, and metal electrode. Kwak *et al.*[13] have calculated the interface state density from the hysteresis in the capacitance-voltage characteristic due to electronic charge trapping in BST thin films prepared by RF magnetron sputtering with Pt electrodes. An interface state density of $2\sim3\times10^{12}$ cm$^{-2}$ was calculated for an as deposited sample. A post top electrode anneal at 650°C for 30 s in $O_2$ or $N_2$ decreased the interface state density by one third and was accompanied by a large decrease in leakage indicating interface trap density may play a roll in determining the effective Schottky barrier height for thermionic emission in BST thin films. The trap density at the Pt/BST interface, and its variation with annealing condition, remains to be determined for our films.

**Table 1.** Schottky barrier heights as a function of annealing condition

| *Annealing condition* | *Barrier height (eV)* | *Applied voltage (volts)* |
|---|---|---|
| As deposited | 0·67 | 1·4 |
| 550°C 15 min $O_2$ | 1·29 | 1·6 |
| 550°C 15 min $O_2$ + 400°C 20 min FG | 0·92 | 2·2 |
| 550°C 15 min $O_2$ + 400°C 20 min FG + 400°C 20 min $O_2$ | 1·22 | 2·2 |

### 3.2 Relaxation currents

Figure 3 shows the dielectric relaxation (depolarization) currents after various annealing conditions for 30 nm MOCVD BST. A 1 volt step was applied to the sample for 1000 s, the capacitor shorted, and the depolarization currents measured. The relaxation currents are seen to follow a power law dependence known as the Curie–von Schweidler law, $J(t) = J_o t^{-n}$.[14] The exponent in the power law depends on the annealing conditions being approximately 0·99 for the as deposited and oxygen annealed films and decreases to 0·92 after annealing at 400°C for 20 min in forming gas. The magnitude of the relaxation current was relatively insensitive to the initial oxygen anneal of 550°C for 15 min, but subsequent anneals in oxygen at 550°C have shown a decrease in relaxation currents.[15] The forming gas anneal had the most pronounced affect, increasing the relaxation currents by an

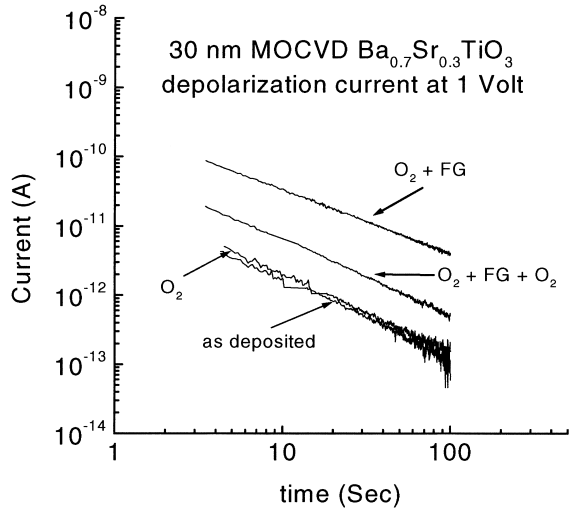


**Fig. 3.** Dielectric relaxation currents for 30 nm MOCVD BST with Pt electrodes under different annealing conditions. As deposited, annealed at 550°C for 15 min in $O_2$, subsequent anneal at 400°C for 20 min in forming gas, and re-annealed at 400°C for 20 min in $O_2$.

**Table 2.** Charge loss after 1 s due to relaxation currents

| *Annealing* | a ($fF/\mu m^2$)$S^{n-1}$ | n | C/A(f = $1/t_{write}$) ($fF/\mu m^2$) *at 1 Volt* | % $Q_{lost}$ |
|---|---|---|---|---|
| As deposited | 0·23 | 0·99 | 55·2 | 12·9 |
| 550°C 15 min $O_2$ | 0·26 | 0·99 | 80·2 | 10·6 |
| 550°C 15 min $O_2$ + 400°C 20 min FG | 2·76 | 0·92 | 60·8 | 60·1 |
| 550°C 15 min $O_2$ + 400°C 20 min FG + 400°C 20 min $O_2$ | 0·73 | 0·99 | 73·3 | 28·3 |

order of magnitude. Other reducing ambients have shown less impact on the magnitude of the relaxation currents. Annealing MOCVD BST thin films in a $N_2$ ambient at 550°C for 15 min only slightly increases the relaxation currents.[15] Further studies are needed, such as controlled $O_2$ partial pressure anneals, to determine whether the increase in the relaxation currents is caused by a reduction effect or by the presence of $H_2$. Re-annealing the sample at 400°C for 20 min in $O_2$ reduced the relaxation currents by about 20%.

### 3.3 Charge loss mechanisms

The slow polarization currents in BST thin films are a charge loss mechanism that must be considered in addition to the D.C. leakage through the film.[16–18] Only polarization components that are able to respond within the read/write times projected for future DRAMS ($t_{write} \approx t_{read} \leq 10\ ns$) result in usable charge storage. Polarization components that cannot respond within the read/write time result in charge loss. The worst case charge loss due to dielectric relaxation occurs during the first read after a refresh time following a write to the opposite state for a capacitor that has been continually written to the same logic state for many refresh cycles.[18] Numata *et al.*[18] have calculated the charge loss due to the dielectric relaxation current for the case of the power law exponent $n = 1$. However, a range of values of $n$ may be observed for MOCVD BST films[19] and $n$, as discussed above, may change with annealing condition. The fraction of charge loss occurring following the first write to the opposite logic state for a capacitor that has been in the same logic state for a long time (steady state condition), and $n < 1$, can be estimated by calculating the ratio of usable free charge (free charge on the capacitor plate that has not been compensated by slow polarization currents) after a refresh time, to the initial usable charge just following the opposite state write

$$Q_{\text{lost}} = 1 - \frac{Q_{\text{usable}}(t_{\text{refresh}})}{Q_{\text{usable}}(t_{\text{write}})} \approx \frac{2a(t_{\text{refresh}})^{1-n} - (t_{\text{write}})^{1-n})}{C(1/t_{\text{write}})(1-n) + a((t_{\text{refresh}})^{1-n} - (t_{\text{write}})^{1-n})} \quad (2)$$

$a$ and $n$ are the magnitude and exponent of the power law relaxation current defined by, $J_R(t) = aVt^{-n}$, and $C(1/t_{write})$ is the capacitance density measured at a frequency of $1/t_{write}$. For $t_{write} \leq 10\ ns$, this frequency is in the low microwave region. BST thin films have been shown to follow the power law dispersion up to the low microwave region.[19,20] $Q_{lost}$ gives the fraction of charge lost due to the slow polarization currents after a refresh time for the case of writing to the opposite state. In deriving eqn (2) the capacitor has been assumed to be perfectly isolated and the leakage currents through the film have been neglected. In addition, the relaxation currents are assumed linear which, for the range of operating voltages projected for future DRAMs ($Vcc \leq 2V$), is a good approximation. Table 2 shows the estimated charge loss due to the relaxation currents for 30 nm MOCVD BST capacitors with an area of $10^4\ \mu m^2$ under different annealing conditions assuming $V_{cc} = 2$ volts (and half of $V_{cc}$ is dropped across the capacitor), $t_{write} = 10\ ns$, and $t_{refresh} = 1$ s. The charge loss varies from about 10·6% in the first oxygen anneal to a maximum of 60% for the forming gas anneal. It is important to note that the calculated charge loss due to dielectric relaxation is for large ($10^4\ \mu m^2$) unpassivated planar capacitors and may not reflect the charge loss for submicron BST capacitors in actual DRAM circuits. It is interesting to compare the loss due to the relaxation currents to that due to leakage for 30 nm MOCVD BST capacitors with a steady state leakage of $\approx 2\times10^{-9}\ A\,cm^{-2}$ and $C/A = 70 - 80\ fF\,\mu m^{-2}$ (first and last oxygen anneal). The voltage drop (proportional to charge loss) can be estimated by $\Delta V \approx J\Delta t/(C/A)$ which gives a drop of about 0·03% for $V_{cc} = 2$ Volts with a refresh time, $\Delta t$, of 1 s. This is well below the charge loss due to dielectric relaxation.

## 4 Conclusion

We have investigated the leakage and dielectric relaxation currents of MOCVD $Ba_{0.7}Sr_{0.3}TiO_3$ thin films after post top electrode anneals in oxygen and forming gas (95% Ar, 5% $H_2$). The effective barrier height for thermionic emission of electrons

from the cathode varied from 0·67 to 1·29 eV depending on annealing conditions. The forming gas had the most pronounced affect on the relaxation currents, increasing the magnitude of the relaxation currents by a factor of ten. Re-annealing in oxygen at 400°C for 20 min improved the leakage but still resulted in an estimated 28% charge loss due to the slow polarization currents for the large unpassivated planar capacitors used in this study. Additional annealing studies are needed to determine if the relaxation currents and charge loss can be further reduced after forming gas anneals.

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